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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,103	12/11/2003	Takeshi Osada	0553-0387	9163

7590 07/20/2006

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,103	OSADA, TAKESHI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: Page 7, line 25 to page 8, line 11 of the specification reference Figures 5A to 5E, however, the specification should be referencing Figures 6A to 6E.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7 and 9 recite the limitations "said plurality of gate lines" and "said plurality of source lines." There is insufficient antecedent basis for these limitations in the claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al. (JP 2000-047255) in view of Koyama (US 2001/0040565).

Regarding claim 1, Kaneko et al. disclose an image display device comprising:

a plurality of pixels which are arranged in matrix (Drawing 3 shows pixels arranged in a matrix, each pixel containing a transistor 15, a capacitor C_{stg} and C_{LC}.);

a plurality of data signal lines (Drawing 3, S1-Sn);

a plurality of scanning lines (Drawing 3,V1-Vn);

a first driver circuit which controls the data signal lines (Drawing 3 and paragraph [0022] explain that signal line drive circuit 17 controls the data lines S1-Sn.); and

a second driver circuit which controls the scanning lines (Drawing 3 and paragraph [0021] explains that scan signal drive circuit 18 controls the scanning lines V1-Vn.), and

a testing circuit comprising a plurality of AND circuits connected in series (Drawing 3 and paragraph [0023] explain that pixel defective checking circuit 20 contains a plurality of AND circuits connected in series with each other.);

wherein each of the plurality of data signal lines is connected to each of input portions of the plurality of AND circuits (Drawing 3 shows that each signal line S1 through Sn being connected to inputs of the AND circuits A1 through An-1.);

wherein an output portion of the testing circuit is connected to a testing terminal (Drawing 3 shows that the output of the testing circuit is DIV, which is a detection terminal for testing for pixel defects as explained in the end of paragraph [0027].) and

an input portion of the testing circuit is connected to a power source (Drawing 3 shows that the input portion on the testing circuit starting at AND circuit A1 is connected to Vref.), and wherein the first driver circuit and the plurality of pixels are connected to the testing circuit through the data signal line (Drawing 3 shows that signal line drive circuit 17 and the pixels are connected to test circuit 20 through signal lines S1-Sn.).

Kaneko et al. fail to teach a testing circuit comprising a plurality of NAND circuits connected in series.

Koyama discloses of a testing circuit using a plurality of NAND circuits (Figure 4, NAND circuits 9403-9405.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to replace the AND circuits taught by Kaneko et al. with the NAND circuits with the buffers comprising 3 inverters taught by Koyama such that the logical equivalent of the AND circuit would be kept while using NAND circuits in order to provide a buffer before the result from the NAND circuit is output to the next NAND circuit.

Regarding claim 2, Kaneko et al. and Koyama disclose a image display device according to claim 1.

Koyama also discloses wherein an electronic device mounting the image display device is any one of a laptop personal computer, a portable information terminal, a video camera, a cellular phone, a digital camera (Figure 12).

Regarding claim 3, Kaneko et al. disclose a testing method of an image display device:

a plurality of pixels which are arranged in matrix (Drawing 3 shows pixels arranged in a matrix, each pixel containing a transistor 15, a capacitor C_{stg} and C_{LC}.);

a plurality of data signal lines (Drawing 3, S1-Sn);

a plurality of scanning lines (Drawing 3,V1-Vn);

a first driver circuit which controls the data signal lines (Drawing 3 and paragraph [0022] explain that signal line drive circuit 17 controls the data lines S1-Sn.); and

a second driver circuit which controls the scanning lines (Drawing 3 and paragraph [0021] explains that scan signal drive circuit 18 controls the scanning lines V1-Vn.), and

a testing circuit comprising a plurality of AND circuits connected in series (Drawing 3 and paragraph [0023] explain that pixel defective checking circuit 20 contains a plurality of AND circuits connected in series with each other.);

wherein each of the plurality of data signal lines is connected to each of input portions of the plurality of AND circuits (Drawing 3 shows that each signal line S1 through Sn being connected to inputs of the AND circuits A1 through An-1.);

wherein an output portion of the testing circuit is connected to a testing terminal (Drawing 3 shows that the output of the testing circuit is DIV, which is a detection terminal for testing for pixel defects as explained in the end of paragraph [0027].) and an input portion of the testing circuit is connected to a power source (Drawing 3 shows that the input portion on the testing circuit starting at AND circuit A1 is connected to

Vref.), and wherein the first driver circuit and the plurality of pixels are connected to the testing circuit through the data signal line (Drawing 3 shows that signal line drive circuit 17 and the pixels are connected to test circuit 20 through signal lines S1-Sn.), and

wherein a testing pulse is inputted to the testing circuit and a square wave signal is supplied to an output portion of the testing terminal in accordance with the testing pulse (Drawing 4 shows that the output of terminal DIV is a square wave.).

Kaneko et al. fail to teach a testing circuit comprising a plurality of NAND circuits connected in series.

Koyama discloses of a testing circuit using a plurality of NAND circuits (Figure 4, NAND circuits 9403-9405.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to replace the AND circuits taught by Kaneko et al. with the NAND circuits with the buffers comprising 3 inverters taught by Koyama such that the logical equivalent of the AND circuit would be kept while using NAND circuits in order to provide a buffer before the result from the NAND circuit is output to the next NAND circuit.

Regarding claim 4, Kaneko et al. and Koyama disclose a testing method of an image display device according to claim 3:

Kaneko et al. also disclose wherein the testing pulse is outputted to the data signal line in accordance with the input of a video signal (Drawing 4 shows the testing

pulse represented by Vref is output in correspondence with the input to signal lines S1-Sn, i.e. the input video signal, as explained in paragraph [0027].).

Regarding claim 5, Kaneko et al. and Koyama disclose a testing method of an image display device according to claim 3:

Kaneko et al. also disclose wherein the testing pulse is a High signal in all the data signal lines and is switched sequentially into a low signal (Drawing 4 shows that the testing pulse Vref is a high signal and that the scanning lines V1-Vn are sequentially scanned and a low signal is output if a pixel effect is obtained.).

Regarding claim 6, Kaneko et al. and Koyama disclose a testing method of an image display device according to claim 3:

Kaneko et al. also disclose wherein the testing pulse is inputted simultaneously to the NAND circuits connected in series (Drawing 3 shows that Vref is simultaneously input to the NAND circuits A1-An-1.).

Regarding claim 7, please refer to the rejection of claim 1, and furthermore Kaneko et al. disclose that the plurality of scanning lines extend orthogonally to said plurality of data signal lines (Drawing 3) and that said plurality of pixels are surrounded by said plurality of scanning lines and said plurality of data signal lines (Drawing 3, the pixels are surrounded by signal lines S1-Sn and scan lines V1-Vn.).

Regarding claim 8, this claim is rejected under the same rationale as claim 2.

Regarding claim 9, please refer to the rejection of claim 3, and furthermore Kaneko et al. disclose that the plurality of scanning lines extend orthogonally to said plurality of data signal lines (Drawing 3) and that said plurality of pixels are surrounded by said plurality of scanning lines and said plurality of data signal lines (Drawing 3, the pixels are surrounded by signal lines S1-Sn and scan lines V1-Vn.).

Regarding claim 10, this claim is rejected under the same rationale as claim 4.

Regarding claim 11, this claim is rejected under the same rationale as claim 5.

Regarding claim 12, this claim is rejected under the same rationale as claim 6.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

11 July 2006

AMR A. AWAD
PRIMARY EXAMINER